UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,119	12/17/2003	Hiroshi Kuroda	XA-10006	5995

181 7590 08/09/2005

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
NGUYEN, DILINH P	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/737,119	KURODA ET AL.	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egawa (U.S. Pat. 6777797).

Egawa discloses a semiconductor device having:

a wiring substrate 10; a chip 16; and

a memory chip 12 or 22, said chip and said memory chip being mounted over the upper surface of said wiring substrate, wherein said chip is constructed of a multiport structure including an interface between it and the inside of said system including said memory chip and an interface between it and the outside of said system, respectively, wherein said memory chip is constructed so as to be accessed to the outside of said system via said microcomputer chip, and wherein said chip 16 is mounted over said wiring substrate 10 in a state being stacked over said memory chip 12 or 22 (fig. 2A, column 5, lines 61 et seq.).

Egawa does not explicitly disclose the chip 16 is a microcomputer chip.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the memory chip is a microcomputer chip in order to use in particular application.

- Regarding claims 2 and 4, Egawa discloses that the chip 16 is connected to first electrodes 30 of said wiring substrate 10 via a plurality of bonding wires 38, said memory chip is connected to second electrodes 30 of said wiring substrate via a plurality of bonding wires 20 or 40, said first electrodes are arranged at the outer periphery side of said wiring substrate from said second electrodes, and the outer dimensions of said chip 16 are equal to or larger than those of said memory chip 22 or 12 (fig. 2A).
- Regarding claim 3, Egawa discloses that the memory chip 22 is formed with a flash memory (fig. 2A, column 6, lines 17-18).
- Regarding claim 5, Egawa discloses that a spacer 15 is interposed between said chip 22 and said memory chip 12 (fig. 2A).
- Regarding claim 6, Egawa discloses a semiconductor device having a System in Package structure in which a system is constituted of:

a wiring substrate 10; a chip 16; and two memory chips 12 and 22, said chips being mounted over the upper surface of said wiring substrate 10, wherein said chip 16 is constructed of a multiport structure including an interface between it and the inside of said system including said two memory chips 12 and 22 and an interface between it and the outside of said system, respectively, wherein each of said two memory chips 12 and 22 is constructed so as to be accessed to the outside of said system via said microcomputer chip, and wherein said two memory chips are mounted over said wiring substrate 10 in a state that one of them is stacked over the other and said chip 16 is

mounted over said wiring substrate 10 in a state of being stacked over said two memory chips 12 and 22 (fig. 2A, column 5, lines 61 et seq.).

Egawa does not explicitly disclose the chip 16 is a microcomputer chip.

However, it would have bee obvious to one having ordinary skill in the art at the time the invention was made to form the memory chip is a microcomputer chip in order to use in particular application.

- Regarding claim 7, Egawa discloses that the chip 16 is connected to first electrodes of said wiring substrate 10 via a plurality of bonding wires 38, the memory chip as the lower layer of said two memory chips is connected to second electrodes of said wiring substrate via a plurality of bump electrodes 20, the memory chip as the upper layer thereof is connected to third electrodes of said wiring substrate via a plurality of bonding wires 40, and said first electrodes are arranged at the outer periphery side of said wiring substrate from said second and third electrodes (fig. 2A).
- Regarding claim 8, Egawa discloses that wherein one of said two memory chips is formed with a ROM, and the other is formed with a flash memory (fig. 2A, column 6, lines 17-18).
- Regarding claim 9, Egawa discloses that the lower surface of said wiring substrate 10 is formed with a plurality of bump electrodes 46 constructing external connection terminals (fig. 2A).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN

LONG PHAM
PRIMARY EXAMINER